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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/329,156 | 06/09/1999 | ZHIJUN QU | IR-1677 | 7761 |

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| EXAMINER | |
|---|---|
| HU, SHOUXIANG | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 08/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/329,156 | QU ET AL. | |
| | Examiner | Art Unit | |
| | Shouxiang Hu | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-4 and 9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

1. In response to the appeal board's decision of Paper No. 27 issued on July 21, 2004, and in view of applicant's Reply Brief of Paper No. 24 filed on June 16, 2003, the finality of the final rejections set forth in the 05-21-02 Office action of Paper No. 19 is withdrawn, and PROSECUTION IS HEREBY REOPENED. New rejections are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama (EP 0118921 A2) in view of Ishimura (US 6,207,993), or, in the alternative, as being unpatentable over Ishimura in view of Akiyama.

Akiyama discloses a semiconductor device (Figs. 2-4, a vertical power MOSFET), comprising: a silicon substrate (1); a first layer (12; $n^-$); a second layer (13; n); and, a plurality of p-type diffusions (3) distributed uniformly with respect to each other into the surface of the second layer, defining p-n junctions therein, and being separated by invertible channels in the second layer, wherein the resistivity in the second layer is lower than that of the first one, as the impurity concentration in the second layer is higher than that in the first layer, and the thickness of the first layer is greater than that of the second one (see page 5, lines 3-13).

Although Akiyama does not explicitly disclose that the doping impurities are uniformly distributed within each of the first and second layers, it is noted that the first and second layers in Akiyama are doped during epitaxial growth, and the only mentioned change of the flow rate of phosphene for the doping in Akiyama occurs between the ending of the growth of the first layer and the starting of the growth of the second layer (see page 5, lines 7-9). Accordingly, the epitaxially grown first and second layers in Akiyama are regarded as inherently having a first and second concentrations of doping impurities uniformly distributed in the first and the second layers, respectively. And, the first and second uniform concentrations of doping impurities then inherently result in uniform resistivity in the first and second layers, respectively.

Akiyama further teaches that one of the main objectives of making the semiconductor device is to provide the vertical power MOSFET with a low on-resistance, and that it is important to reduce the on-resistance as much as possible (page 3, lines 3-8).

Akiyama does not disclose that each of the plurality of p-type diffusions is formed within the second layer.

However, Ishimura teaches to form a vertical power MOSFET (see Fig. 1; also see Fig. 15, and col. 9, lines 30-50) having a plurality of p-type diffusions (3) distributed uniformly with respect to each other into the surface of the second layer (12; $n^+$) which overlies a first layer (2; $n^-$), wherein the plurality of p-type diffusions (3) are formed within the second layer. Ishimura further teaches that (see col. 11, lines 11-20), by forming the plurality of p-type diffusions within the second layer, the vertical power MOSFET can have an on-resistance lower than the on-resistance of a vertical power MOSFET (shown in Fig. 18) in which the plurality of p-type diffusions extending from the second layer (12) into the first layer (2; also see col. 4, lines 29-58). In addition, Ishimura also teaches (see col. 11, lines 21-25) to add a breakdown suppression feature, i.e., a deep diffusion region (11A), at the center of the vertical power MOSFET and its periphery (see Fig1. 1, 2 and 15; also see col. 10, line 46-65), for the purpose of maintaining high breakdown voltage (see col. 11, lines 21-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the plurality of p-type shallow base diffusions of Ishimura, along with (or without) the breakdown-suppression feature, into

the semiconductor device of Akiyama, so that a device with lowered on-resistance suitable for applications that require high breakdown voltage (or not-too-high breakdown voltage) would be obtained.

Or, in the alternative, claims 1-4 and 9 are unpatentable over Ishimura in view of Akiyama, as explained below:

As discussed above, the semiconductor device disclosed in Ishimura (see Figs. 1, 2 and 15, also see col. 10, line 46-65) comprises: a first layer (2; $n^-$) on a semiconductor substrate (1); a second layer (12; $n^+$); a plurality of p-type diffusions (3) distributed uniformly with respect to each other into the surface of the second layer (12; $n^+$), wherein the plurality of p-type diffusions (3) are within the second layer (12). Accordingly, Ishimura discloses the claimed invention defined in claims 1-4 and 9, except that Ishimura does not expressly disclose that the semiconductor substrate is formed of silicon and the doping impurities are uniformly distributed within each of the first and second layers.

However, one of ordinary skill in the art would readily recognize that silicon substrate is commonly used as the semiconductor substrate for forming power MOSFET devices with a well developed and commonly used silicon process as evidenced in Akiyama (see page 5, lines 1-2); and that, as also evidenced in Akiyama (see page 5, lines 3-13), the method of epitaxial growth is one of the few commonly used methods for forming high quality multiple semiconductor layers having different doping impurity concentrations, as it provides good control on the layer thickness and

the doping impurity concentrations therein. As discussed before, the epitaxially grown first and second layers naturally have a first and second concentrations of doping impurities uniformly distributed in the first and the second layers, respectively.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the silicon substrate and the epitaxially grown first and second layers of Akiyama into the semiconductor device of Ishimura, so that a vertical power MOSFET would be obtained with a commonly used silicon process and with high quality in the first and second layers. And, in each of such epitaxially grown first and second layers, the doping impurity concentration and the resistivity would then be naturally uniform.

***Response to Arguments***

2. Applicant's arguments in the 02-19-02 Amendment of Paper No. 18 with respect to claims 1-4 and 9 have been considered but are moot in view of the new ground(s) of rejection.

3. Applicant's arguments in the 01-28-03 Appeal Brief of Paper No. 22 have been fully considered but they are not persuasive, as explained below.

First, it is noted that appellant's arguments regarding Yamamoto (US 5, 521,410) have been considered but are moot in view of the withdrawal of the portion of obviousness claim rejections based on Akiyama in view of Yamamoto, as mentioned in Section 6 above.

Appellant's main arguments regarding the obviousness claim rejections based on the combination of Akiyama and Ishimura include:

(A). Akiyama and Ishimura cannot be combined to obtain the subject matter of claim 1 in that Akiyama requires the base regions to extend into a low conductivity region, which teaches away from the claimed invention of claim 1 (see the bottom paragraph in page 4 through the second paragraph in page 5 in the Brief).

(B). One skilled in the art would not be directed by Ishimura to modify Akiyama to include base regions that are wholly contained within a low resistivity layer in that such a modification without more (such as addition of regions 11A) would not achieve a desirable outcome (see the third paragraph in page 6 through the bottom of page 7 in the Brief).

These arguments have been fully considered but they are not persuasive, as explained below.

With respect to Arguments A and B above, as discussed in the obviousness claim rejections above, Akiyama discloses a vertical power MOSFET (see Fig. 2), which teaches the claimed invention of claims 1-4 and 9, except that the base diffusion regions (3; i.e., the plurality of diffusions) in Akiyama are not wholly contained within the high conductivity second layer (13). However, Ishimura teaches that a vertical power MOSFET device shown in Fig. 18 with the base diffusion regions (3 and 11) being extended from the high conductivity second layer (12) into the low conductivity first layer (2) has an ill-effect on the on-resistance, increasing the on-resistance (see col. 4, lines 53-58). To avoid such ill-effect on the on-resistance and to further lower the on-

resistance, Ishimura expressly teaches to form the base diffusion regions (3) wholly contained within the high conductivity second layer (12), as shown in Fig. 1 (also see col. 11, lines 11-29). In addition, Ishimura also teaches (see col. 11, lines 21-25) to add a breakdown-suppression feature, i.e., a deep diffusion region (11A), at the center of the vertical power MOSFET and its periphery (see Fig1. 1, 2 and 15; also see col. 10, line 46-65), for the purpose of maintaining high breakdown voltage (see col. 11, lines 21-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the a plurality of p-type shallow diffusions of Ishimura into the semiconductor device of Akiyama, in order to further lower the on-resistance. And, with the breakdown-suppression feature being added, the character of high breakdown voltage would also be obtained.

Moreover, it is noted that much of the arguments in Arguments A and B above, especially in Argument A, are arguments against the references individually; and that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, although Akiyama teaches to form the vertical power MOSFET (Fig. 2) with the base diffusion regions (3) being extended into the low conductivity first layer (12) for maintaining high breakdown voltage (see page 4, lines 21-29), Akiyama does not support or suggest the assertion that forming the base diffusion regions wholly within the high conductivity second layer would always result in an unacceptably low

breakdown voltage. Even without the teachings of Ishimura, one of ordinary skill in the art would readily recognize that the depth of the base diffusion regions is an art-recognized result-oriented variable that directly affects the on-resistance, as admitted by Appellant (see the paragraph starting with "Ishimura et al." in page 7 of the Brief); and that lower on-resistance can be desirably and readily obtained by reducing the depth of the base diffusions for certain applications which requires very high current but with not-too-high or medium breakdown voltage. Based on the combined teachings of Akiyama and Ishimura, the artisan would readily realize that, with the base diffusion regions extended into the low conductivity first layer, Akiyama' device would still have a relatively high on-resistance due to the ill-effect on the on-resistance identified by Ishimura (col. 4, lines 52-58). Ishimura concurs with Akiyama on that the extension of the base diffusion regions into the low conductive first layer helps to maintain high breakdown voltage (see col. 3, lines 14-27, in Ishimura). However, after identifying the ill-effect on the on-resistance associated with the extension of the base diffusion regions, Ishimura provides a remedy to overcome the ill-effect and to further lower the on-resistance (see col. 11, lines 11-25). Accordingly, the teachings of Ishimura do not contradict to the teachings of Akiyama; instead, the former manifest an improvement to the later. And the artisan would be encouraged by Ishimura to modify Akiyama's device in order to overcome that ill-effect so as to further reduce the on-resistance, while still maintaining its high breakdown voltage.

In addition, with respect to Argument A above, it is further noted that Akiyama's discusses on the correlation between the breakdown voltage and the resistivity and/or

the resistivity limit of the high resistivity drain region (see page 2, lines 22-27) is provided to explain the drawbacks of a vertical power MOSFET in which the base diffusion regions are entirely formed in the single high resistivity drain region. Thus such a discussion is not particularly relevant to the vertical power MOSFET in which the single high resistivity drain region is already replaced with a high conductive second layer and a low conductivity (i.e., high resistivity) first layer underlying the second layer.

In argument A, Appellant also asserts that "Akiyama proposes extending the bottom of each base region into the high resistivity layer 12, so that the depletion layers caused by the reverse voltage may expand and link up, rather than concentrate on the corners of the base regions to cause breakdown" (see the top paragraph of page 5 in the Brief). However, this assertion is not fully supported in Akiyama. Akiyama clearly explains that, in the vertical power MOSFET shown in Fig. 2, "the breakdown voltage is primary determined in the lower parts of the well regions 3" (see page 4, lines 28-29). And the lower parts therein apparently include not just the bottom of the well regions (3) but also the lower corners of the well regions (3), as shown in Fig. 2, since the depleted region (D) conforms and covers each of the lower corners. Following the natural trend admitted by Appellant that the electric field lines are heavily concentrated around the corners of the base regions (see the bottom paragraph of page 4 in the Brief), the breakdown voltage in the vertical power MOSFET of Fig. 2 in Akiyama should then still be primary determined in the lower corners of the well regions (3).

In further response to Argument B above, contrary to Appellant's allegation that "Ishimura et al. teaches that disposing the base regions within a low resistivity layer is

undesirable" (see the bottom paragraph of page 7 in the Brief), forming the base regions within the low resistivity layer (see layer 12 in Fig. 1 of Ishimura; i.e., the high conductivity second layer) is the main feature advocated by Ishimura (see col. 11, liens 11-20) for overcoming the ill-effect on the on-resistance associated with the base regions being extended into the low conductivity first layer (see Fig. 18 and col. 4, lines 53-58). Moreover, Ishimura also teaches to add a breakdown suppression feature, i.e., a deep diffusion region (11A) added at the center of the vertical power MOSFET and its periphery (see Fig1. 1, 2 and 15; also see col. 10, line 46-65), for the purpose of maintaining high breakdown voltage (see col. 11, lines 21-25). Therefore, the artisan would be encouraged and directed by Ishimura to modify the device of Akiyama by forming the base diffusion regions within the high conductivity second layer in order to achieve a desirable outcome of lower on-resistance, or, by also adding the breakdown suppression feature of Ishimura in the device, in order to achieve a desirable outcome of lower on-resistance and high breakdown voltage.

In view of the above discussions, it is also apparent that, in the alternative, the instant invention defined in claims 1-4 and 9 are obvious over Ishimura in view of Akiyama, because it would be obvious for the artisan to form the vertical power MOSFET of Ishimura by forming the first and second layers through epitaxial growth on a silicon substrate, as taught in Akiyama. The artisan would be motivated to do so, since, as evidenced in Akiyama, the artisan would readily recognize that silicon substrate is the most commonly used substrate in the industry and that the method of epitaxial growth is one of the few commonly used method for forming high quality

multiple semiconductor layers having different doping impurity concentrations. The artisan would still be motivated to do so, even though Akiyama teaches to form the base diffusion regions extending into the low conductivity first layer, because the artisan would readily recognize that the epitaxial growth method would always result in high quality in the first and second layer, regardless whether or not the base diffusion regions are wholly within the second layer, as the first and second layers would always be formed prior to the formation of the base diffusion regions, and also because the artisan would always be fully aware of the drawbacks in the device of Akiyama and the remedy to it, based on the thorough teachings in Ishimura.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
August 6, 2004

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